

# ELECTROCHEMICAL ANALYSIS OF GRAPHENE NANOPARTICLE AND ACTIVATED CARBON COMPOSITE FOR FLEXIBLE ENERGY STORAGE APPLICATIONS

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## Article Info



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## Abstract

This study presents the development of a foldable/rollable supercapacitor utilizing symmetrical electrode architecture. The active material comprises a composite of graphene flakes ink and activated carbon paste, with a dense metal mesh functioning as the current collector. A locally sourced “Malmal” fabric, impregnated with H<sub>3</sub>PO<sub>4</sub> and PVA serves as the separator. The supercapacitive characteristics of the device, driven by a non-Faradaic charge storage mechanism, confers it with exceptional charge storage capacity and power density, rendering it highly effective for applications necessitating rapid power delivery. The device's charge-discharge dynamics were scrutinized under applied biases of 1.7 V and 1 V, both in the absence of a load and with a 1.1-ohm load resistor, over varied temporal intervals. EIS analysis was employed to elucidate the device's electrical properties, yielding Nyquist and Bode plots. The RESR and parallel connected R<sub>p</sub> were determined to be 2.048 Ω and 4.312 Ω, respectively. The relatively low R<sub>p</sub> value indicates the device's suitability for interfacing with loads exhibiting impedances lower than R<sub>p</sub> and its potential for integration in cascaded configurations with other supercapacitors to augment overall charge storage capacity. It has been observed that the understudy fabricated supercapacitor device capacitance varies from 3.58 uF to 7.74 μF, by approximating  $Z[\Omega] \approx X_c$  in the formula  $C = 1/2\pi f X_c$ , over the range of frequencies from 10 mHz to 10 kHz having biasing range varies from 0.1 V to 1.7 V.

## Keywords:

Graphene Composite, Flexible supercapacitor (SC), Fabric based separator, Charging-Discharging characteristics, Electrochemical characteristics.

## Introduction

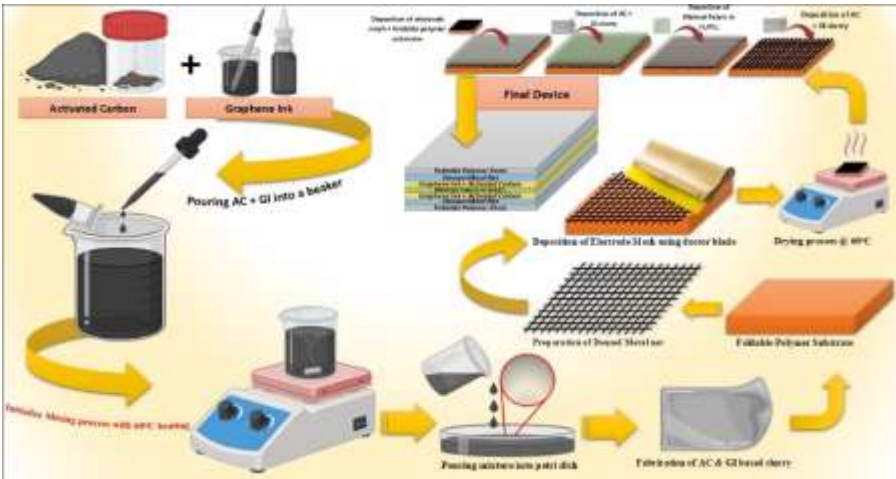
Flexible energy storage systems are an emerging field of research, with a focus on creating lightweight, flexible, and durable devices for integration into portable and wearable electronics [1-3]. Traditional batteries face limitations due to their low power density, while capacitors are restricted by low energy density [4,5]. To address these challenges, supercapacitors (SCs) have been developed as a hybrid energy storage solution, offering a balance between the capacitors (high-power density) and batteries (high energy density). The key components of supercapacitors—highly porous active electrode materials, separators, electrolytes, and current collectors—significantly influence the device's electrochemical performance [6-9]. Depending on the method of charge storage Supercapacitors are divided into three categories: (a) Electrical Double Layer Capacitors (EDLCs) that rely on non-Faradaic charge storage, (b) Faradaic Capacitors (FCs) which depend on redox reactions, and (c) Hybrid Capacitors that combine both Faradaic and non-Faradaic charge storage processes [10,11]. EDLCs store charge through electrostatic separation at the electrode-electrolyte interface without involving chemical reactions. When a voltage is applied, opposite charges accumulate on the electrode surfaces, forming an electric double layer with a nanoscale separation. This creates a high capacitance due to the large surface area of porous electrodes and the small charge separation distance, enabling rapid energy storage and release. Solid-state supercapacitors have already found commercial applications, demonstrating the practical viability of this technology [12,13,14]. With the continuous advancements in flexible and wearable electronics for diverse applications, it is imperative that energy storage solutions exhibit flexibility, cost-efficiency, reliability, and compatibility with emerging energy generation technologies such as Piezoelectric/Triboelectric Nanogenerators (TENGs) and photovoltaics. The charge storage capability of a supercapacitor (SC) is inherently linked to the properties of the electrode material [15]. One of the most effective strategies to enhance capacitance is through the development of highly porous, electrochemically active nanoscale electrode materials. Two-dimensional materials, such as graphene and its derivatives, are ideal candidates due to their exceptional electrochemical properties and maximal surface-to-volume ratio [16,17]. The intercalation of graphene nanoscale clusters, in conjunction with activated carbon (AC), can significantly improve overall charge storage capacity when used as an active electrode material. Furthermore, a mesh-like structure in the current collector enhances electrolyte infiltration, ensuring that all active sites (functional groups) within the electrode material are fully utilized. Likewise, the permeability of the separator plays a crucial role in reducing leakage currents, thereby preserving maximum charge accumulation at the interface of electrode/electrolyte to ensure a consistent supply of energy during the discharge cycle [18]. To engineer stretchable devices that exhibit capacitive behavior for energy storage, diverse materials and structural configurations can be employed. Extensive research in the literature explores various approaches, such as reduced graphene oxide (rGO)-based flexible micro-supercapacitors (FPMSCs), fabricated via photolithography, which are designed as micro-power sources for next-generation on-chip electronics [19]. While these devices demonstrate favorable capacitive behavior, they are often limited in delivering high power and energy densities under real-time operational loads. Similarly, aqueous suspensions of graphene incorporated into activated carbon electrodes can function as conductive additives with optimized particle size distribution. Notably, R.E. Williams et al. have exceeded the capacitance limits of conventional activated carbon-based electrodes by utilizing a planar structure, where a few-layer graphene intercalation was introduced during electrode fabrication. This method increased the potential window to 1.2 V, achieving improved cyclic stability and a better retention ratio within the same voltage range,

following the electric double-layer capacitor (EDLC) approach, while minimizing equivalent series resistance (ESR) to 3 Ω [21]. However, planar approaches reported in the literature frequently encounter limitations, such as lower charge/discharge current densities, suboptimal capacitance values, constrained potential windows, and high self-discharge rates due to leakage currents.

To address these challenges, we employed a straightforward yet more effective and cost-efficient method by incorporating a dense metal mesh, which significantly enhances the effective surface area of the electrode while simultaneously functioning as an improved current collector. A malmal cloth impregnated with H<sub>3</sub>PO<sub>4</sub> and PVA serves as an efficient separator between the electrodes, facilitating the passage of electrolytes through its pores. The fabrication process, surface structure, and elemental composition of the materials utilized were characterized using SEM, EDS and XRD. The device's charge-discharge behavior was analyzed using a data acquisition system, and the results were plotted using Origin software to examine its performance under applied biases of 1.7 V and 1 V for varying time intervals. Additionally, Electrochemical Impedance Spectroscopy (EIS) was conducted, presenting Nyquist and Bode plots to investigate crucial parameters of the Randles cell, such as Equivalent Series Resistance (R<sub>ESR</sub>), parallel-connected self-discharge resistance (Rp), and equivalent capacitance (Ceq), all of which determine the operational efficiency of the device under study.

**Experimental:**

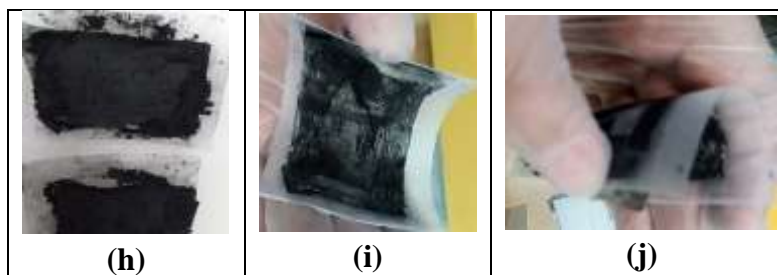
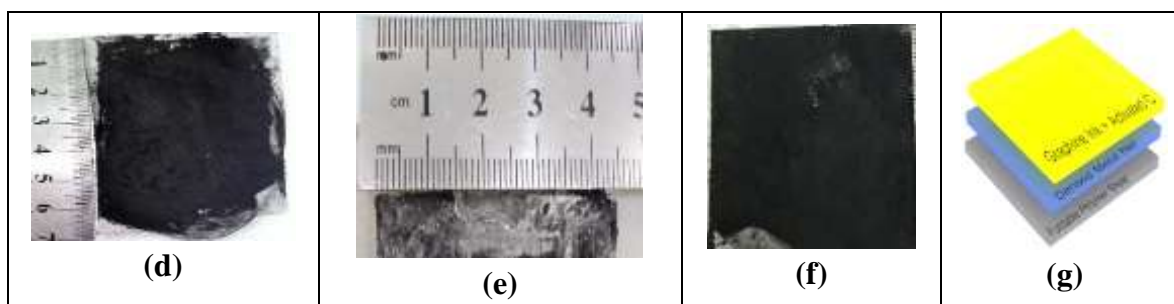
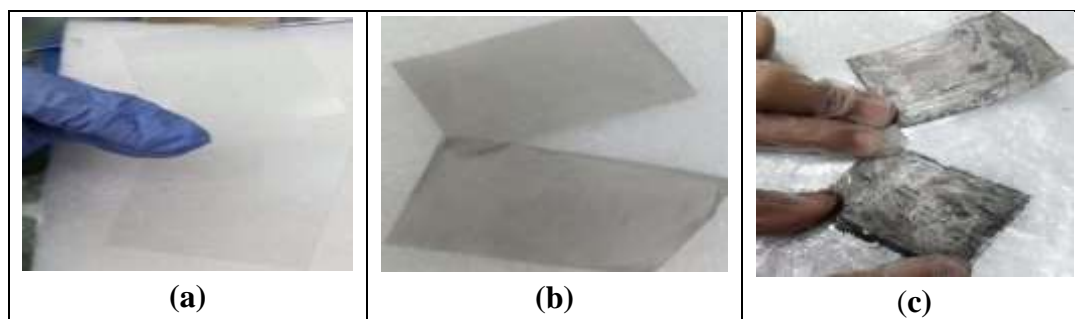
All chemicals utilized in the current research were of pure industrial grade and utilized without any further processing. The chemicals include Poly vinyl alcohol (PVA, 99.99%, Sigma-Aldrich, USA), Activated Carbon (AC, 99.99%, Sigma-Aldrich, USA), Graphene flakes in water (C, 7440-44-0, Alfa Aesar, UK), and Ortho-phosphoric acid (H<sub>3</sub>PO<sub>4</sub>, 99.99%, Merck, Germany). For the fabrication of the rollable supercapacitor, symmetric configuration of electrode has been adopted. The fabrication process of a single electrode and device is outlined as follows.

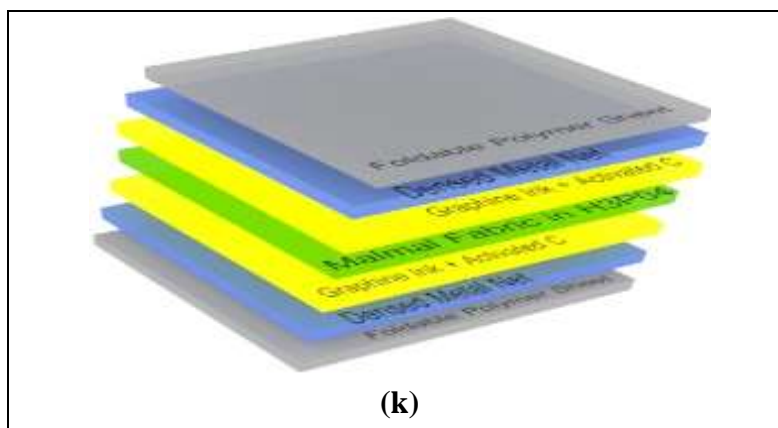


**Figure 1: Schematic illustration of the entire process from material to device fabrication.**

For the synthesis and fabrication of the proposed supercapacitor, a polymer sheet as the base/ supporting substrate for the electrode Figure 2(a), and a dense metal mesh Figure 2(b), were cut into 6.5 cm x 4.5 cm structures Figure 2(d, e), and adhered together by using carbon double tape to serve as the current collectors Figure 2(c). Cu wire leads were attached to each metal mesh to establish Ohmic contacts at the

edges to define the cathode and anode. The electrode material was prepared by mixing activated carbon (0.4 g) with graphene flakes ink without any binder, which was formulated by dispersing graphene (0.125 g) in deionized (DI) water (5 mL). After achieving a homogeneous slurry, the Doctor Blade method was employed to ensure a uniform coating of the active material onto the metal mesh Figure 2(f), forming the single electrode structure: "Polymer sheet/Metal mesh/Graphene flakes ink-AC composite" Figure 2(g). The same procedure was replicated to fabricate the second symmetric electrode, resulting in a mirror configuration: "Graphene flakes ink-AC composite/Metal mesh/Polymer sheet" Figure 2(h). The polymer sheet functioned as a flexible supporting substrate, contributing to the mechanical stability of the device while having no direct influence on its electrochemical performance as demonstrated by the foldability and rollability illustrated in Figure 2(i, j). To prevent short-circuiting, thin insulating paper sheets were placed over the exposed areas of both electrodes. A locally sourced fabric known as "Malmal" was selected as the separator, soaked in  $\text{H}_3\text{PO}_4$  and PVA (1 mL acid in 10 mL PVA) solution to act as the electrolyte and separator was placed between the two electrodes, completing the device's structure arranged as: "Polymer sheet/Metal mesh/Graphene flakes ink-AC composite/Paper separator soaked in  $\text{H}_3\text{PO}_4$ /Malmal fabric soaked in  $\text{H}_3\text{PO}_4$  and PVA / Graphene flakes ink-AC composite/Metal mesh/Polymer sheet". Finally, the assembled device was folded and rolled, with copper wire leads serving as connections to each electrode. A graphical representation of the complete layered structure is shown in Figure 2(k). This design highlights the flexibility of device and suitability for energy storage in rollable or foldable configurations.





**Figure 2:** Steps to fabricate the graphene flakes ink based foldable supercapacitor: (a) Flexible polymer sheet demonstrating foldability and rollability, (b) Dense metal mesh, (c) Metal mesh adhered to the polymer sheet, (d) Length specification of the metal mesh, (e) Width specification of the metal mesh, (f) Application of the graphene flakes-ink and activated carbon paste over the metal mesh, (g) Schematic representation of a single electrode, (h) Fabricated symmetric electrodes for the supercapacitor, (i, j) Demonstration of the foldability and rollability enabled by the electrode configuration, (k) Structural schematic of the complete fabricated device.

Following the physical fabrication of the stretchable/flexible graphene flakes ink-based hybrid supercapacitor matrix, the Scanning Electron Microscopy (SEM), Energy Dispersive Spectroscopy (EDS), X-ray Diffraction (XRD) will be done to analyze the surface structure and elemental composition of the materials employed in device construction. The charging and discharging currents were analyzed through a data acquisition system, and the resulting data was processed using Origin software to examine the device's charge-discharge behavior. Additionally, Electrochemical Impedance Spectroscopy (EIS) analysis was conducted to obtain Nyquist and Bode plots, which were used to evaluate the effective  $R_p$  and  $R_{ESR}$  values of the supercapacitor. For XRD, (Analytical X'Pert<sup>3</sup>-Powder), SEM (KYKY-EM-6900) and EIS (BST8-KJ- potentiostat) system was used.

## Results and Discussion:

### Structural Analysis:

The XRD patterns of standalone graphene flakes, activated carbon (AC), and their composite reveal distinct structural characteristics as shown in Figure 3. Graphene exhibits a sharp (002) peak at  $\sim 26.5^\circ$ , indicating a crystalline structure with well-ordered layers. In contrast, AC shows a broad peak around  $22^\circ$ – $25^\circ$ , signifying its amorphous nature with disordered carbon structures. The composite maintains an amorphous structure, resembling AC, with no distinct graphene peak, suggesting high dispersion of graphene. These findings align with literature, where activated carbon/graphene composites typically show broad peaks around  $23^\circ$ , confirming turbostratic disorder. The structural features observed support their applications in energy storage, adsorption, and catalysis.



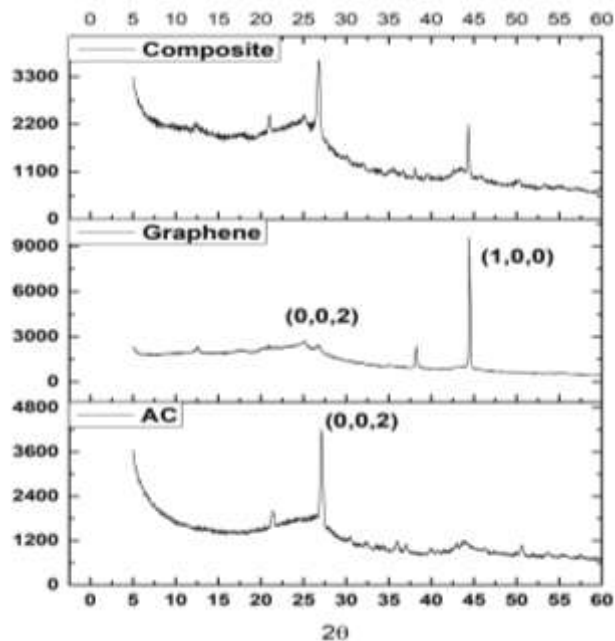
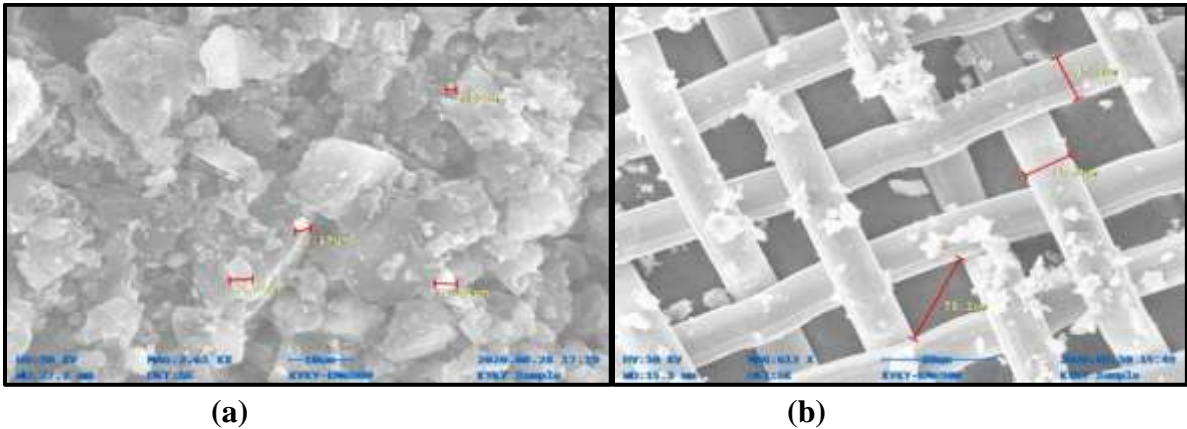
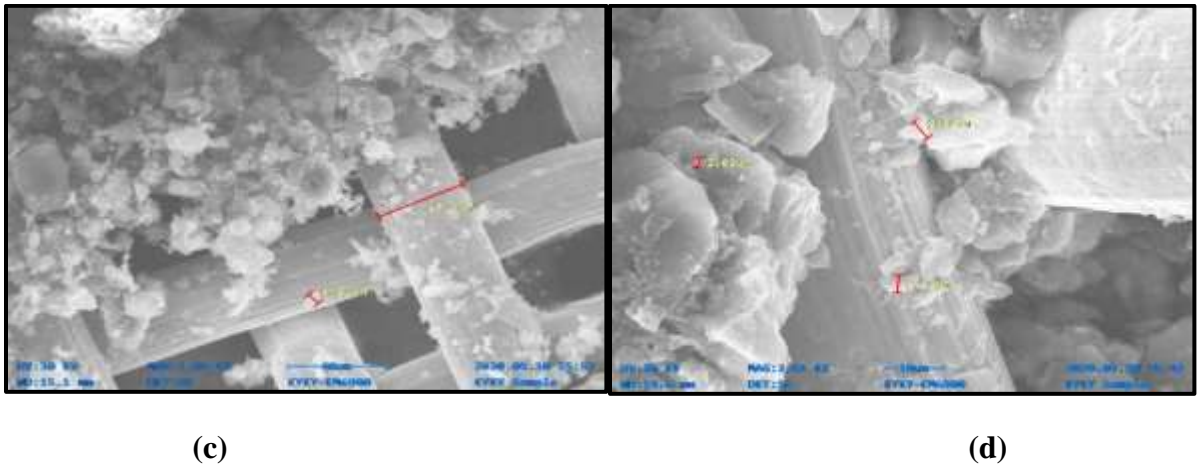


Figure 3: Diffraction pattern of AC, Graphene and its composite.

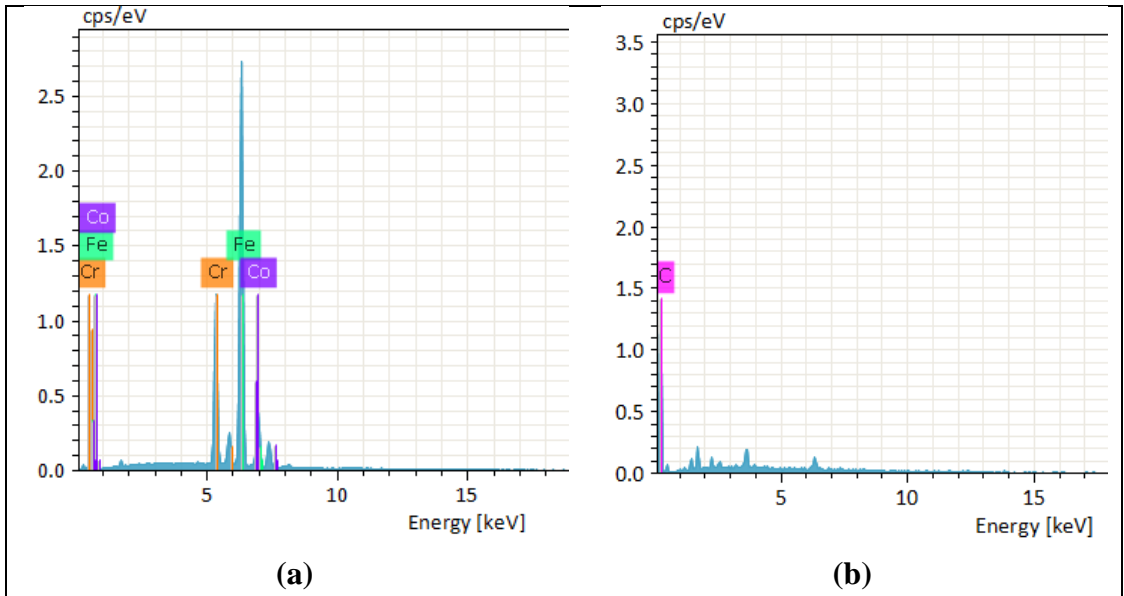
Surface Morphological Imaging:

To achieve higher capacitance, it is crucial to select materials that offer an extensive surface area, as demonstrated in Figure 4(a). In this study, the composite made by mixing activated carbon with graphene flakes-ink offers a larger surface area, which significantly improves the device's charge storage capacity. SEM images illustrate various stages of the fabrication process, including the dense metal net serving as the current collector, activated carbon deposited on the net, and the composite paste of graphene flakes-ink and activated carbon applied to the structure (Figure 4(b), (c), and (d)). The spacing between the consecutive bars of the dense metal net is measured to be approximately 37 microns, while distance between two strands, i.e., pore size in mesh is less than 75 microns (Figure 4(b)), providing the necessary porous architecture to maximize the surface area and thus, capacitance. To achieve a high surface area, that is essential to get improved capacitance, SEM images provide clear evidence that the selected material offers the requisite porous structure. This increased surface area facilitates greater charge storage, aligning with the capacitance equation  $C=(A*\epsilon)/d$ . The observed porosity in the material confirms its potential to enhance charge storage capabilities, directly contributing to improved performance of the SC device.





**Figure 4:** SEM imaging illustrating (a) The rough surface morphology of activated carbon (AC), (b) The dense metal net serving as the current collector, (c) Activated carbon (AC) layered over the dense metal net, and (d) The paste formed by mixing graphene flakes-ink and activated carbon applied to the dense metal net.



**Figure 5:** EDS analysis a) EDS plot of dense metal net, b) Active Material’s Energy Dispersive Spectroscopy

Similarly, the EDS, shown in Figure 5(a), display the EDS spectrum of the dense metal mesh, which serves as the current collector for our device. Figure 5(b) displays the elemental composition for the material utilized in the formation of electrode. The EDS analysis of the active material reveals a predominance of the carbon element, confirming that the materials utilized for electrode fabrication are indeed carbon-based.

**Electrical Characterization:**

Electrical tests were carried out to study the charging and discharging behaviors of the device. A Data Acquisition Unit was used to track and record the charging current values for a given bias over set time periods. Similarly, it sampled the discharging current values under both no-load conditions and when

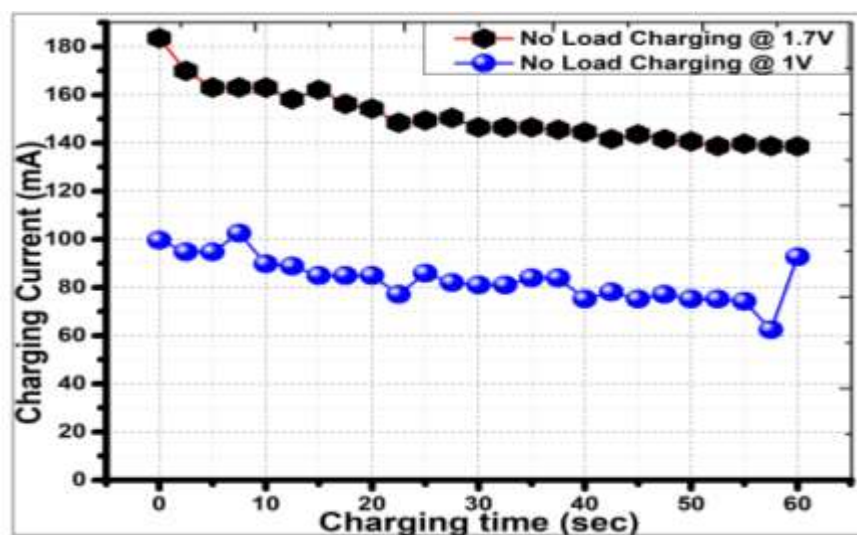
subjected to a load (1.1-ohm resistor). The fabricated device was charged at voltages of 1.7 V and 1 V, followed by discharging under no load and through the 1.1-ohm load resistor alternately. In this section, the curves representing charging and discharging currents are analyzed to elucidate the operational behavior of the fabricated device.

### Charge / Discharge Characteristics:

The device was first charged without any load by applying a 1.7 V voltage for 1 minute. The charging current during this phase is shown in Figure 6(a), exhibited an exponential decline from an initial peak value of 183.59 mA to a reduced value of 138.67 mA. Subsequently, the discharging behavior of the device was examined using a 1.1-ohm load resistor, achieved by connecting four 5W, 4.7  $\Omega$  resistors in parallel. During the discharging phase, as illustrated in Figure 6(b), the discharging current decreased from 70.31 mA to 8.79 mA over approximately 5.4 minutes. Following this, the fabricated device was allowed to undergo self-discharge.

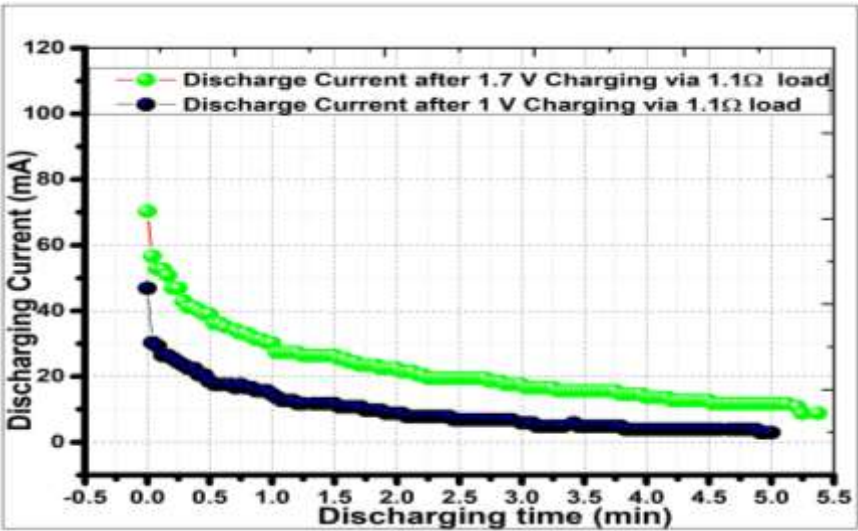
The same experimental procedure was replicated to investigate the behavior of the device at an applied voltage of 1 V under no-load conditions. By applying the Bias voltage of 1 V for 1 minute, as shown in Figure 5(a), the charging current displayed a similar exponential decay pattern, reducing from 99.61 mA to 92.77 mA. Figure 6(b) illustrates the discharging current behavior through the 1.1-ohm load resistor over a period of 5 minutes. The discharge current commenced at 46.8 mA and subsequently decreased to 2.93 mA. Following this discharge cycle, the device was left in an idle state for an extended duration to ensure complete discharge, thereby optimizing its readiness for future utilization. Notably, the discharge current exhibited a decline from a higher initial value to a lower final value, consistent with the behavior observed in capacitors and batteries i.e., conventional energy storage devices.

Further, it has been observed that having the higher value of charging bias will enable the device to have both higher charging current and higher discharging current at every instant of time as depicted in Figure 6(a, b).



(a)

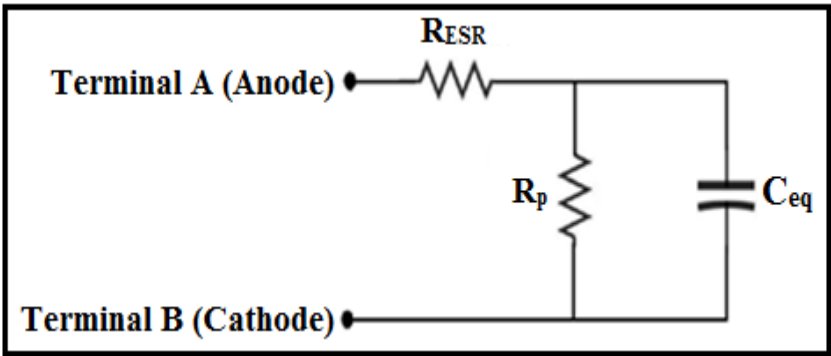




(b)

**Figure 6:** Charging and discharging behavior @ 1.7 V and @ 1 V DC bias. (a) Charging current behavior without any load. (b) Discharging current behavior via load of 1.1-ohms following charging at both 1.7 V and at 1 V.

Based on the Randles model of the supercapacitor [21], two critical parameters can effectively characterize the behavior of the fabricated device: the ( $R_p$ ) and  $R_{ESR}$ , as illustrated in Figure 7. For optimal device performance, the  $R_{ESR}$  should be minimized (approaching zero), while the  $R_p$  should be maximized (ideally infinite) [23]. These parameters were determined through Electrochemical Impedance Spectroscopy (EIS) analysis using both Nyquist and Bode plots.



**Figure 7:** Randles circuit model of Supercapacitor

**EIS Analysis:**

In EIS analysis, by using the Galvano-static mode i.e., current through the device is kept constant but applied DC potential (0.1V – 1.7V). An alternating signal of fixed amplitude 100 mV<sub>ac</sub> will be superimposed over range of DC biases (0.1V – 1.7V). And for each bias, the range of frequency for superimposed alternating signal will be 10 mHz-10 kHz. Nyquist plots ( $Z_{Real}$  versus the negative of  $Z_{Im}$ ) were created for each DC bias value (0.1 V to 1.7 V), which represents different charging biases. Figure 8 shows a comparison of the Nyquist plots for different charging biases.

Nyquist Plot:

In the Nyquist plot, points on the horizontal axis that are closer to the origin correspond to higher frequencies (kHz), while those positioned further away represent lower frequencies (mHz). At elevated frequencies, the capacitive reactance ( $X_c=1/2\pi fC$ ) diminishes, allowing the current to flow through the path of least resistance, predominantly via the equivalent series resistance ( $R_{ESR}$ ) and capacitance. As apparent from Table 1, at elevated frequencies (kHz), the Nyquist plot clearly reveals the  $R_{ESR}$  values for each charging bias. In contrast, at reduced frequencies (mHz or Hz), the capacitive reactance increases significantly, resulting in current to follow the path with the least resistance. Thus, at these lower frequencies, the current primarily traverses through  $R_{ESR}$  and self-discharge resistance ( $R_p$ ). As a result, in this frequency range, the Nyquist plot reflects values that correspond to the cumulative effect of  $R_{ESR}$  and  $R_p$  [21].

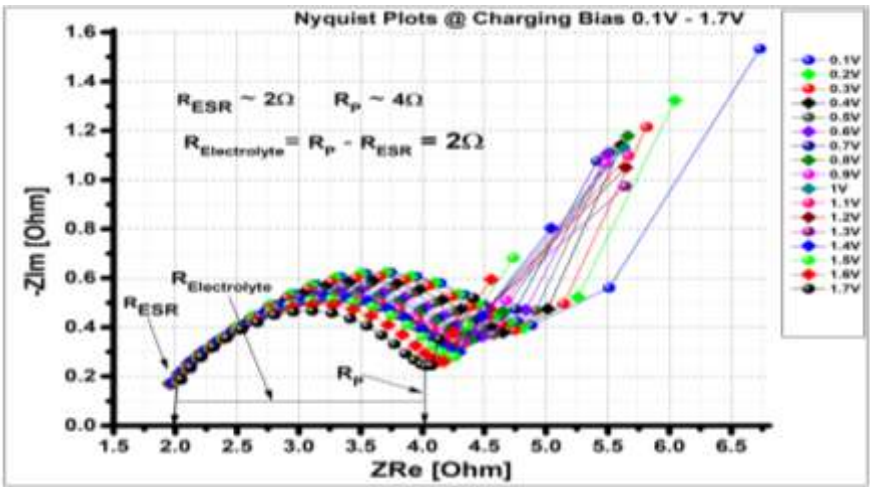


Figure 8: Nyquist Plots @ various Charging Biases (0.1V - 1.7V).

Typically, the self-discharge resistance  $R_p$  values are significantly higher than the equivalent series resistance ( $R_{ESR}$ ) allowing us to approximate the values obtained at lower frequencies as  $R_p$  i.e.,  $R_p \approx R_{p1}$ . Alternatively, a more precise method for determining  $R_p$  involves subtracting the measured  $R_{ESR}$  from each value recorded at various charging biases. This can be mathematically expressed as  $R_p = R_{p1} - R_{ESR}$ , providing an accurate assessment of the self-discharge resistance for the device under investigation.

The magnitude of  $R_{ESR}$ , and magnitude of self-discharge resistance  $R_p$  (Figure 8) are approximately  $2\ \Omega$  and  $4\ \Omega$  respectively, as reported in Table 1, these values are taken at different charging biases from the Nyquist plots. From the real axis of impedance, it is evident that electrolytic resistance  $\sim 2\ \Omega$  for the range of charging biases. The non-linear region is also apparent from the Nyquist plot, in lower frequency regime of the fabricated device, which directed us about the charge storage mechanism during charging procedure. In this low frequency range, if the slope of the diffusive line is short and higher than 45 degrees, that means all active sites are fully accessible to electrolyte ion in a short period of time. It confirms the EDLC i.e., non-Faradaic charge storage mechanism otherwise it refers to Faradaic charge storage mechanism due to the involvement of ionic diffusion in electrolyte [22], which is our case due to the ionic diffusion in electrolyte for range of charging biases (0.1V - 1.7V) from the fabric soaked in Phosphoric acid ( $H_3PO_4$ ).

Table 1: Parameters extracted from Nyquist plot @ various charging biases

Charging Voltage (V)	$R_{ESR}$ (Ohms)	Approximated Self-Discharge Resistance $R_{p1} = R_p + R_{ESR}$ (Ohms) @ lower frequencies	Exact Self-discharge Resistance $R_p = R_{p1} - R_{ESR}$ (Ohms) @ lower frequencies	Electrolytic Resistance $(R_p + R_{ESR}) - R_{ESR}$ (Ohms)
0.1	2.048	6.36	4.312	4.312
0.2	2.014	5.59	3.576	3.576
0.3	2.008	5.71	3.702	3.702
0.4	2.001	5.55	3.549	3.549
0.5	1.987	5.49	3.503	3.503
0.6	1.976	5.43	3.454	3.454
0.7	1.966	5.42	3.454	3.454
0.8	1.965	5.33	3.365	3.365
0.9	1.96	5.32	3.36	3.36
1.0	1.952	5.31	3.358	3.358
1.1	1.975	5.43	3.455	3.455
1.2	1.964	4.76	2.796	2.796
1.3	1.975	4.74	2.765	2.765
1.4	1.99	4.71	2.72	2.72
1.5	2.021	3.88	1.859	1.859
1.6	2.035	3.94	1.905	1.905
1.7	2.048	3.93	1.882	1.882

Bode Impedance Plot:

For analyzing the functionality of the device under test, the Bode Impedance plot has been generated through EIS analysis, across a frequency spectrum ranging from 10 mHz to 10 kHz. In the Bode Impedance (Z) plot, values along the horizontal axis that are closer to the origin correspond to lower frequency ranges (mHz), whereas those positioned further away from the origin indicate higher frequency values (kHz). For each applied direct current (DC) bias (ranging from 0.1 V to 1.7 V), a Bode Impedance plot (Impedance Z [ $\Omega$ ] versus frequency f [Hz]) has been constructed. This plot serves multiple purposes: it enables the determination of the capacitive behavior of the fabricated device, allowing us to ascertain whether it functions effectively as a capacitor. Additionally, it facilitates the measurement of key parameters, including the capacitive reactance ( $X_c$ ), self-discharge resistance ( $R_p$ ) and the equivalent series resistance ( $R_{ESR}$ ) of the device.

Figure 9 presents impedance based Bode plots across the charging biases of 0.1 V to 1.7 V, illustrating the variation in impedance over a range of frequencies. Notably, the data indicates that as the frequency goes up, the impedance goes down and vice versa. This trend strongly supports the desired characteristics of the fabricated SC, confirming its efficacy to be a viable energy storage component.

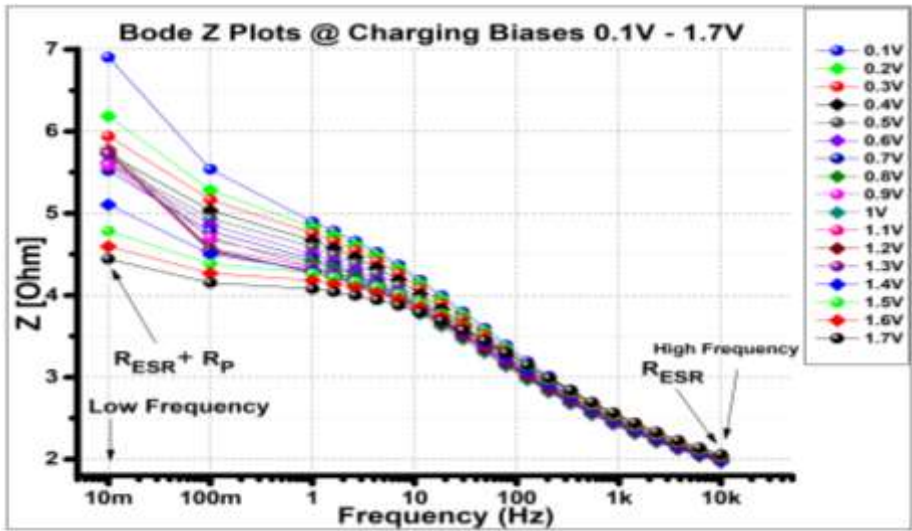


Figure 9: Bode Impedance plots at different biases.

It has been noticed that when the charging voltage is increased, it leads to a notable reduction in the equivalent series resistance ( $R_{ESR}$ ), as detailed in Table 2. Specifically, the  $R_{ESR}$  decreases from 2.056  $\Omega$  at 0.1 V to 1.998  $\Omega$  at 1.4 V. Similarly, for the charging bias range the self-discharge resistance ( $R_p$ ) exhibits a significant decline, dropping from 4.848  $\Omega$  to 2.385  $\Omega$ . The reduction in  $R_{ESR}$  is particularly significant, as it is essential for optimal device performance that this value approaches zero, further corroborating the findings presented in Table 2. This trend highlights the efficacy of fabricated devices in energy storage applications.

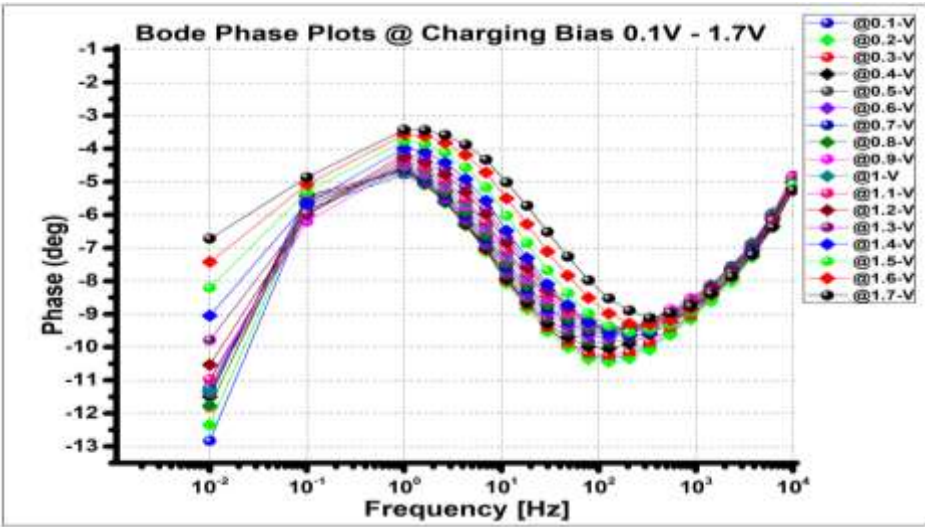
**Table 2:** Summary of parameters derived from the Bode Impedance plot across various charging biases, highlighting the changes in equivalent series resistance ( $R_{ESR}$ ) and self-discharge resistance ( $R_p$ ) at different applied voltages

Charging Voltage (V)	Equivalent Series Resistance $R_{ESR}$ (Ohms) @ higher frequencies	Approximated Self-discharge Resistance $R_{p1}$ (Ohms) @ lower frequencies	Exact Self-discharge Resistance $R_p = R_{p1} - R_{ESR}$ (Ohms) @ lower frequencies
0.1	2.056	6.904	4.848
0.2	2.023	6.188	4.165
0.3	2.016	5.94	3.924
0.4	2.009	5.724	3.715
0.5	1.994	5.627	3.633
0.6	1.984	5.606	3.622
0.7	1.973	5.522	3.549
0.8	1.973	5.784	3.811
0.9	1.967	5.59	3.623
1.0	1.96	5.741	3.781
1.1	1.983	5.772	3.789
1.2	1.971	5.743	3.772
1.3	1.983	5.726	3.743
1.4	1.998	5.106	3.108
1.5	2.029	4.785	2.756
1.6	2.043	4.596	2.553
1.7	2.057	4.442	2.385

**Bode Plot (Phase Analysis):**

For each applied charging bias (0.1 to 1.7 V), corresponding to the charging voltage, Bode Phase plots (Phase versus frequency) were generated over the frequency range of 10 mHz to 10 kHz to visualize the charging phase behaviour. In the Bode Phase plot, the horizontal axis near the origin represents lower frequencies (mHz), while values further from the origin represent higher frequencies (kHz). At these higher frequencies, where the capacitive reactance ( $X_c = 1/2\pi fC$ ) is reduced, the current follows the path of least impedance, flowing through the equivalent series resistance ( $R_{ESR}$ ) and capacitance, represented by  $X_c$ . The angle between the current and charging bias is the phase angle. Initially, the phase difference decreases until it reaches a critical frequency, denoted as 'fc,' after which the phase difference begins to increase again, as illustrated in Figure 10. This critical frequency serves as an indicator of the maximum effective physical area that the supercapacitor can access. Thus, at higher frequencies (kHz), the Bode Phase plot approaches a reduced phase angle, as the current primarily flows through  $R_{ESR}$  and the equivalent capacitance ( $C_{eq}$ ), which ideally acts as a short circuit, leaving only resistive components in the current path for each charging bias.

At lower frequencies (mHz or Hz), the capacitive reactance increases, and the current takes the path of higher impedance through both the  $R_{ESR}$  and the self-discharge resistance ( $R_p$ ). These resistances,  $R_{ESR}$  and  $R_p$ , dominate the behaviour of the device in this lower frequency regime, leading the phase angle to approach another reduced value at the lower end of the frequency spectrum.



**Figure 10: Comparative analysis of Bode Phase Plots at Different Charging Biases (0.1 V – 1.7 V).**

In our experimental analysis, it was noticed that the critical frequency at charging biases of 0.1 - 0.3 V is 127.4 Hz. The phase differences for these voltages are -10.34°, -10.44°, and -10.24°, as shown in Figure 10 and Table 3. So, the maximum effective area will be utilized for the device at 127.4 Hz for these charging biases. Similarly, for other charging biases, the respective critical frequencies and phase differences are presented in Table 3. It was noted that as the charging bias increases, the critical frequency rises while the phase difference decreases. For charging voltage of 1.4 V, the critical frequency rises to 206.9 Hz, with a phase difference of -9.659°. Similarly, at charging bias of 1.6 V the device will have phase difference of -9.317°, with critical frequency value as 336 Hz.



Table 3: Bode phase plot data for different charging biases

Charging Voltage (V)	Critical Frequency (Hz)	Phase-difference (degree)	Charging Voltage (V)	Critical Frequency (Hz)	Phase-difference (degree)
0.1	127.4	-10.34	1	127.4	-9.385
0.2	127.4	-10.44	1.1	127.4	-9.456
0.3	127.4	-10.24	1.2	127.4	-9.453
0.4	127.4	-10.04	1.3	127.4	-9.558
0.5	127.4	-9.8550	1.4	206.9	-9.659
0.6	127.4	-9.696	1.5	206.9	-9.543
0.7	127.4	-9.583	1.6	336	-9.317
0.8	127.4	-9.539	1.7	336	-9.109
0.9	127.4	-9.441			

Capacitance- Frequency (C-F) Analysis:

Capacitance- Frequency (C-F) curve have been plotted Figure 11, by approximating the Bode Impedance values  $Z[\Omega]$  to capacitive reactance  $X_c$  i.e.,  $Z[\Omega] \approx X_c$  in the formula  $C = 1/2\pi fX_c$ , across a range of frequency from 10 mHz to 10 kHz, with voltages ranging from 0.1 V to 1.7 V, the supercapacitor (measuring 6.5 cm by 4.5 cm) shows a capacitance that changes from 3.58 F to 7.74  $\mu$ F.

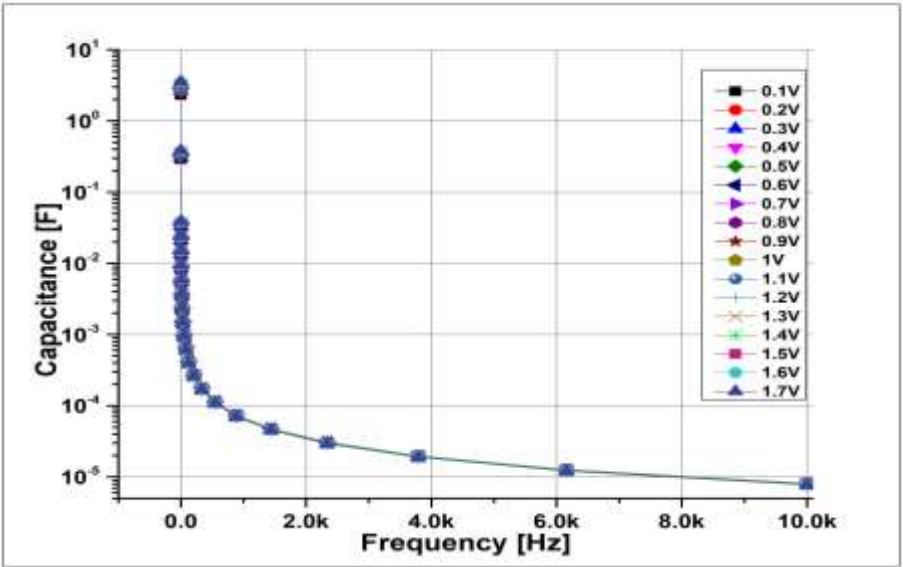


Figure 11: Capacitance- Frequency curve at range of frequency from 10 mHz to 10 kHz at different charging voltages: From 0.1 V to 1.7V.

Figure 11 clearly demonstrates that as the frequency increases, the capacitance decreases, which is consistent with the expected behavior of this type of energy storage device. The analysis was conducted at various biases (0.1V to 1.7V) to capture the supercapacitor's performance during discharge. After charging the device at a fixed bias, such as 1.7V, the voltage gradually drops to zero during discharge. By evaluating the behavior of key parameters such as  $R_{ESR}$ ,  $R_p$ ,  $Z_{Real}$ ,  $-Z_{Imag}$ , and capacitance across a range of charging biases, the analysis over a wide frequency spectrum (10 mHz to 10 kHz) provides insight into the device's behavior. This enables us to identify the optimal operating conditions for maximizing energy extraction from the fabricated supercapacitor during the discharge phase. As shown in Figure 10, increasing frequency causes the capacitance to decrease, which is typical for this kind of energy storage device.

### Conclusion:

The charging-discharging currents for supercapacitor (SC) were meticulously analysed to investigate the functionality. For 1.7 V, the no-load charging current exhibited an exponential decay from 183.59 mA to 138.67 mA within 1 minute. Similarly, during the discharge process through a 1.1-Ohm resistor, the current decreased exponentially from 70.31 mA to 8.79 mA over approximately 5.4 minutes. For no-load, at a lower voltage of 1V, the charging current dropped from 99.61 mA to 92.77 mA in 1 minute. Meanwhile, the current flowing out through the same resistor decreased from 46.8 mA to 2.93 mA over 5 minutes. These results confirm that the fabricated SC provides sufficient backup within the specified period. The Electrochemical Impedance Spectroscopy (EIS) analysis was done using Nyquist and Bode plots, covering a frequency range from 10 mHz to 10 kHz, and voltages range from 0.1 V to 1.7 V revealed a clear super capacitive behaviour. The device exhibited an equivalent series resistance ( $R_{ESR}$ ) of 2.048  $\Omega$  and a self-discharge resistance ( $R_p$ ) of approximately 4  $\Omega$ . As reported in Table 1, the increase in charging voltage led to a decrease in  $R_{ESR}$  from 2.048  $\Omega$  to 1.99  $\Omega$ , and  $R_p$  decreased from 4.312  $\Omega$  to 2.72  $\Omega$ , particularly for the bias range of 0.1 V to 1.4 V. This reduction in  $R_p$  at higher biases indicates an increased self-discharge rate, which could contribute to the device discharging faster than anticipated. The device capacitance was observed to vary between 3.58  $\mu\text{F}$  and 7.74  $\mu\text{F}$ , calculated using the approximation  $Z[\Omega] \approx X_c$  in the formula  $C=1/(2\pi f X_c)$  over the same frequency range, with a biasing range from 0.1 V to 1.7 V. A critical design consideration is that the load impedance must be lower than the self-discharge resistance,  $R_p$ , which in this case is 4  $\Omega$ . If the load impedance exceeds  $R_p$ , most of the charge would flow through  $R_p$  rather than the load, leading to significant energy dissipation within the device and reduced efficiency in energy delivery to the load. This insight is vital for engineers in designing sensors or other devices, ensuring that the load impedance is optimized for effective energy transfer from the SC.

### Declaration of Interest

Authors have no personal or financial benefits that may have affected the work in this paper.

### Author Contribution

Conceptualization; Syed Waqar Shah, S. Fahad. Data curation; M. Shahzad Khan, S. Fahad. Formal analysis; Syed Waqar Shah, S. Fahad, M. Shahzad Khan. Investigation; S. Fahad, M. Shahzad Khan. Methodology; M. Shahzad Khan, S. Fahad. Project administration; Syed Waqar Shah. Resources; Syed Waqar Shah, S. Fahad. Software; M. Shahzad Khan. Supervision; Syed Waqar Shah. Validation; Syed

Waqar Shah, S. Fahad. Visualization; S. Fahad. Writing – original draft; M. Shahzad Khan, S. Fahad. Writing – review & editing; M. Shahzad Khan, S. Fahad.

### **Data Availability**

Relevant data will be made available on request.

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